Features

- ESD Protection for 1 line with Uni-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±20kV (air/contact)
  IEC 61000-4-4 (EFT) 50A (5/50ns)
  IEC 61000-4-5 (Lightning) 7.5A (8/20μs)
  Cable Discharge Event (CDE)
- **Ultra low capacitance: 0.75pF typical**
- For low operating voltage applications: **3.3V**
- **0402 small DFN package** saves board space
- Protect one I/O line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***

Applications

- Antenna applications
- Hand Held Portable Applications
- Data and I/O lines protection
- Analog input lines protection
- Video lines protection
- 3.3V operating systems

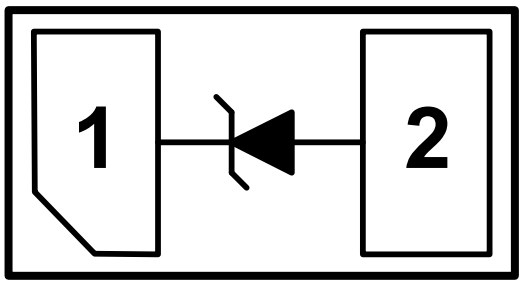
Description

AZ5413-01F is a design which includes a uni-directional ESD rated clamping cell to protect high speed data interfaces in an electronic systems. The AZ5413-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5413-01F is a unique design which includes proprietary clamping cells with ultra low capacitance in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data lines, protecting any downstream components.

AZ5413-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P2E (Bottom View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp=8/20μs)	I_{PP}	7.5	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±20 ±20	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

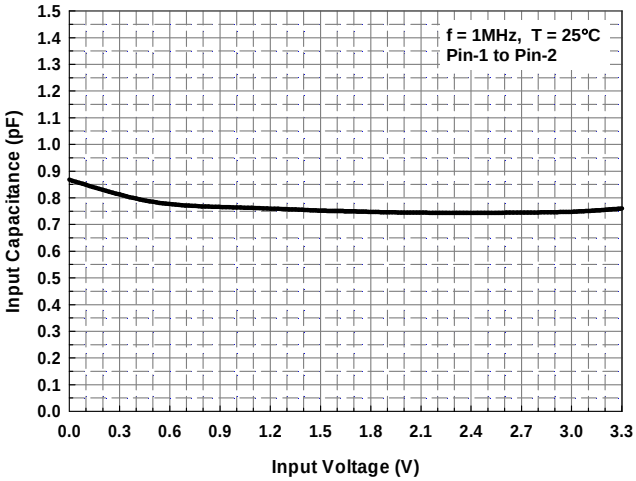
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T = 25°C.			3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 3.3V, T = 25°C, pin-1 to pin-2.			1.0	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25°C, pin-1 to pin-2.	5		7.5	V
Forward Voltage	V_F	I_F = 15mA, T = 25°C, pin-2 to pin-1.	0.6	0.85	1	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = 5A, T = 25°C, pin-1 to pin-2.		5.6		V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T = 25°C, Contact mode, pin-1 to pin-2.		8.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, Contact mode, T = 25 °C, pin-1 to pin-2.		0.2		Ω
Channel Input Capacitance	C_{IN}	V_R = 1.65V, f = 1MHz, pin1-to-pin2, T = 25 °C.		0.75	1	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

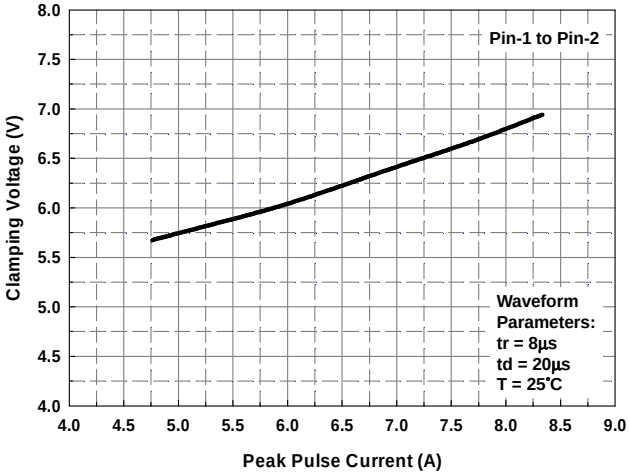
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

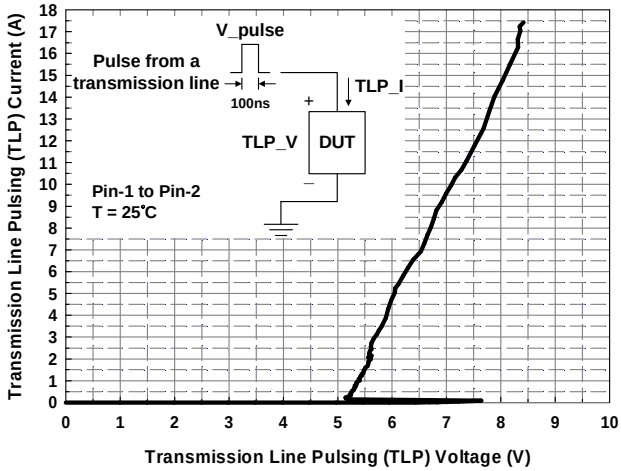
Typical Variation of C_{IN} vs. V_{IN}



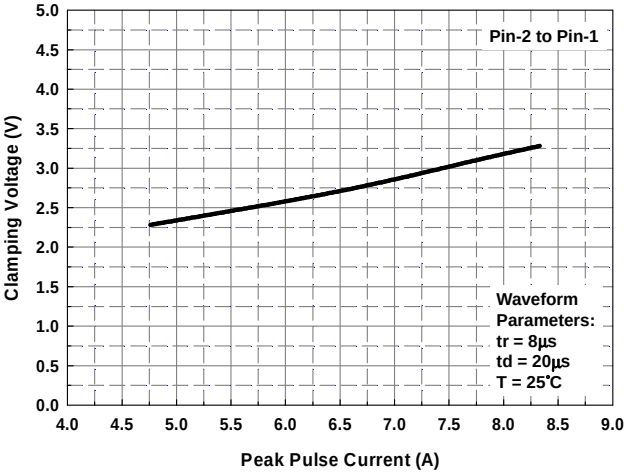
Reverse Clamping Voltage vs. Peak Pulse Current



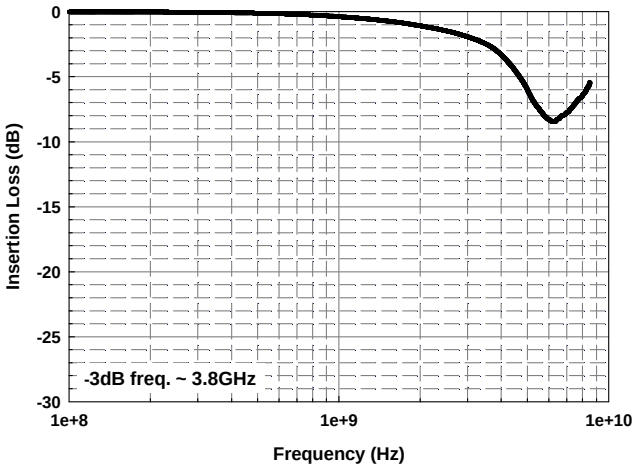
Transmission Line Pulsing (TLP) Measurement



Forward Clamping Voltage vs. Peak Pulse Current



Insertion Loss S21 (I/O-GND)



Applications Information

The AZ5413-01F is designed to protect one line against System ESD / EFT / Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ5413-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ5413-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5413-01F.
- Place the AZ5413-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

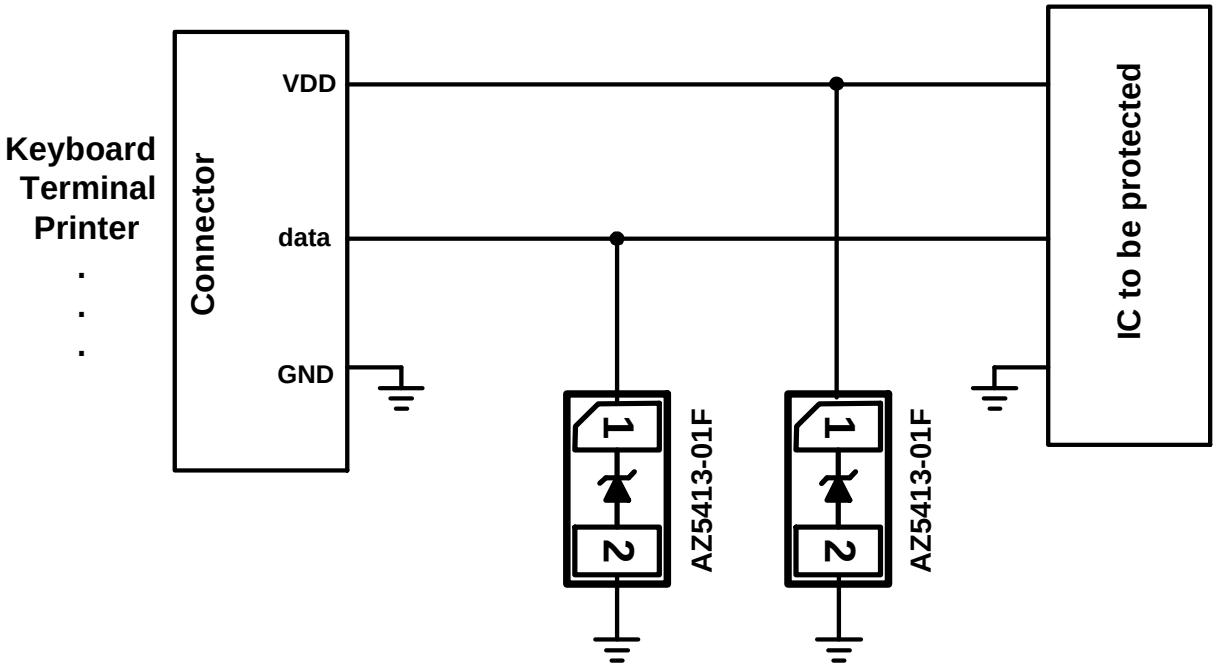


Fig. 1

Fig. 2 shows another simplified example of using AZ5413-01F to protect the control lines, high speed data lines, and power lines from ESD transient stress.

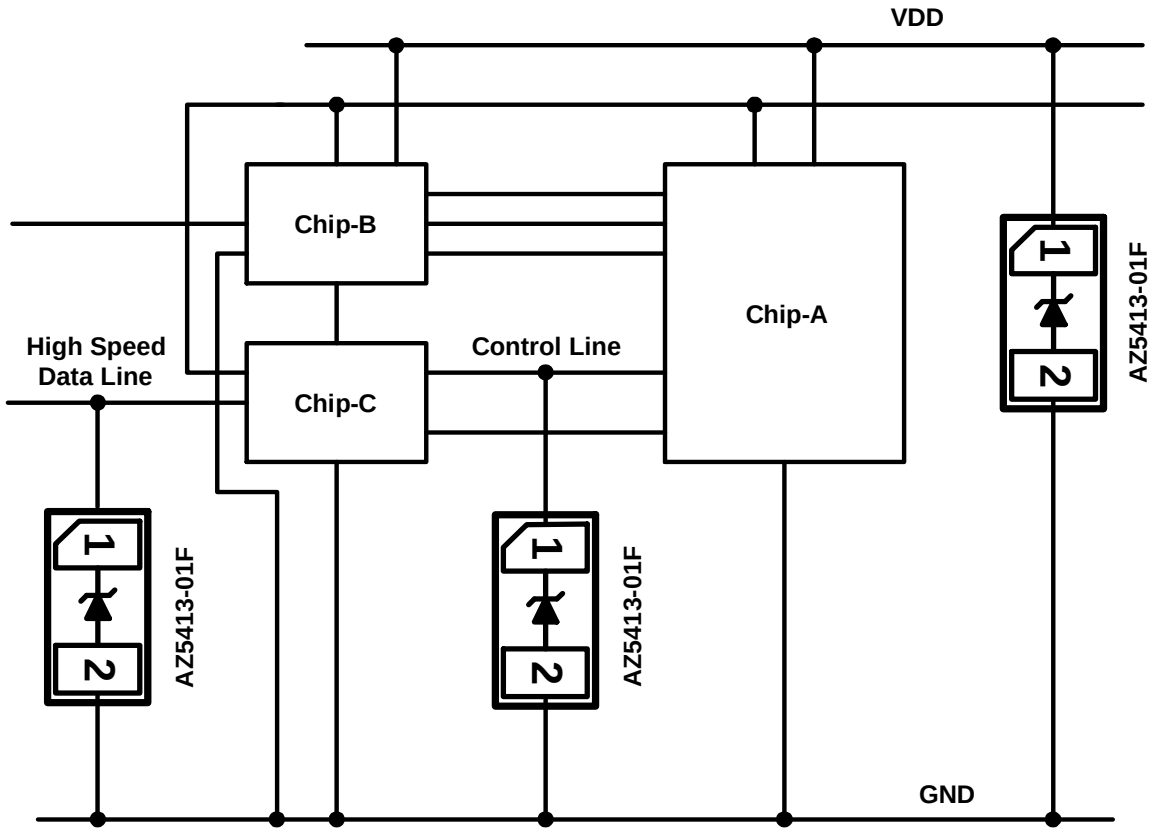
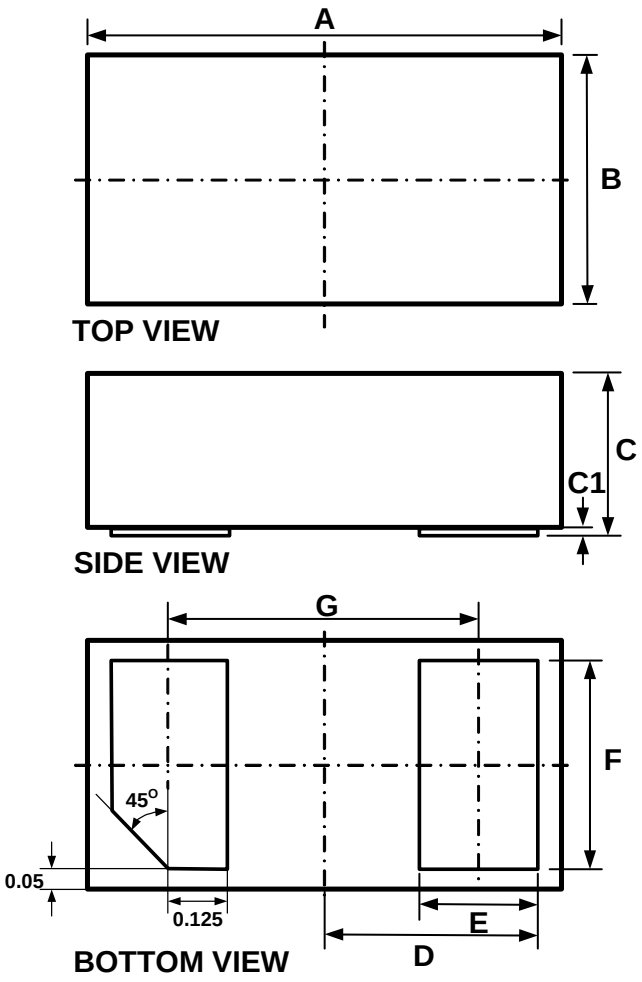


Fig. 2

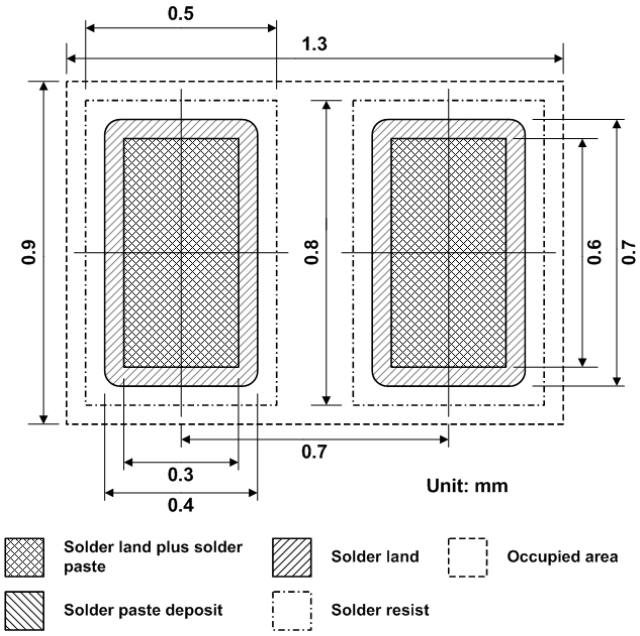
Mechanical Details

DFN1006P2E
PACKAGE DIAGRAMS



Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.45	0.60	0.018	0.024
D	0.45		0.018	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022

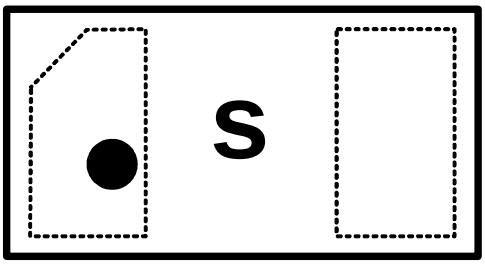
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

Part Number	Marking Code
AZ5413-01F (Green Part)	s

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5413-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reel = 48,000/box	6 box = 288,000/carton

Revision History

Revision	Modification Description
Revision 2014/03/27	Preliminary Release.
Revision 2014/08/20	Update the Marking Code.
Revision 2014/11/04	Update the level of ESD per IEC 61000-4-2.
Revision 2014/11/27	Update the Ordering Information.
Revision 2015/12/07	Formal Release.