ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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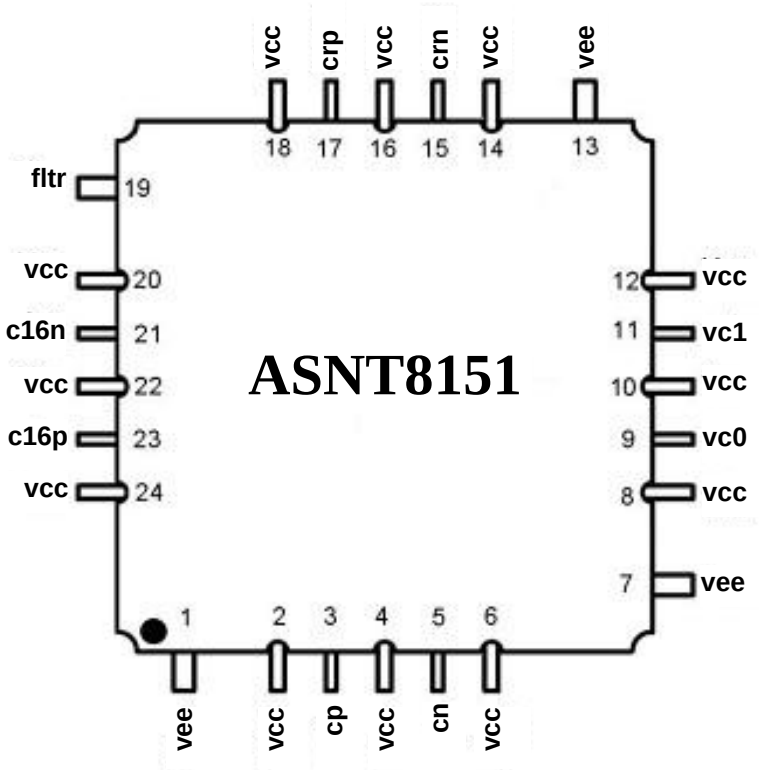
ASNT8151-KMC
24.0-to-32.1*GHz* Programmable PLL with 3 integrated VCOs

- Programmable clock multiplier (CMU) with three selectable frequency ranges of internal PLL
- External RC loop filter
- LVDS input reference clock interface
- Fully differential CML output full-rate clock interface
- Selectable LVDS output clock divided-by-16 interface
- 3-state input control interface
- Single positive or negative power supply
- Power consumption: 0.53*W* at the maximum operational speed
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

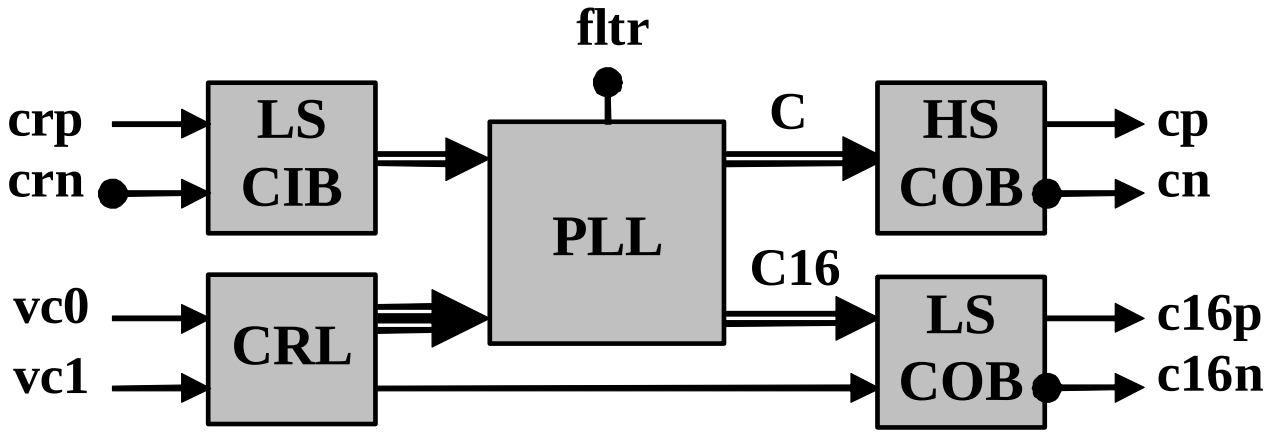

Fig. 1. Functional Block Diagram

ASNT8151-KMC is a clock multiplication unit (CMU) with a triple-range phase-locked loop (PLL) incorporating three high-speed voltage-controlled oscillators: VCO1 (lower frequency), VCO2 (medium frequency), and VCO3 (higher frequency). The chip shown in Fig. 1 generates a high-speed clock signal cp/cn with its phase and frequency locked to those of the incoming reference clock crp/crn. The differential clock cp/cn with frequency *f* is delivered to the output by CML output buffer HS COB. The reference clock crp/crn with frequency *f*/16 is accepted by LVDS input buffer LS CIB. The chip also generates a divided-by-16 clock signal c16p/c16n with frequency *f*/16 that is delivered to the output by LVDS output buffer LS COB. One of the VCOs is activated using two 3-state control signals vc0 and vc1. The same control signals are used to activate or disable the output buffer LS COB.

When operating in closed-loop mode, the PLL requires an external loop filter connected to pin fltr. The PLL also supports an open-loop mode of operation with its selected VCO controlled externally by a voltage applied to the filter pin fltr.

The part's high-speed output buffer supports the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination. The part's low-speed I/Os support the LVDS interface with internal 100*Ohm* termination between the direct and inverted lines. The differential DC signaling mode is recommended for optimal performance.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) can process an external reference clock signal crp/crn with a frequency equal to 1/16 of the selected VCO frequency. The clock inputs support the LVDS logic interface with on chip 100*Ohm* termination between the direct and inverted lines. The proprietary LVDS buffer exceeds the requirements of standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

It is designed to accept a differential signal with a wide range of DC common mode voltages, or a single-ended (SE) signal applied to one input pin with a DC threshold voltage applied to the other input pin. In case of a SE AC-terminated input, the common mode voltage should satisfy the requirements presented in ELECTRICAL CHARACTERISTICS. In case of a SE DC-terminated input, the DC common mode voltage should match the average level of the applied reference clock signal.

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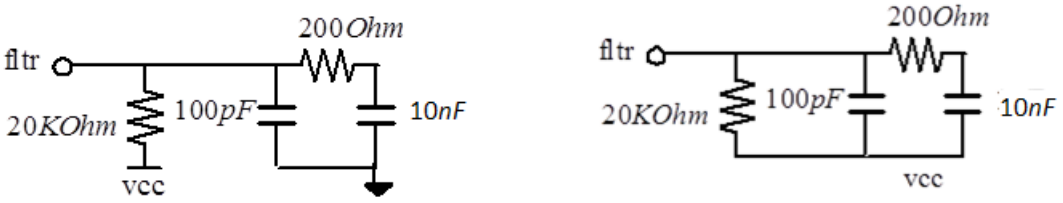
PLL

The PLL contains a phase frequency detector, a charge pump, an on-chip integrator with an additional off-chip filter connected to pin fltr, and three selectable LC-tank VCOs with different central frequencies. The recommended parameters of the external filter schematic components shown in Fig. 2 are for reference only, and can be modified based on specific requirements.



a. b.

Fig. 2. External Filter Schematic for Positive (a) and Negative (b) Power Supplies

The main function of the PLL is to synthesize a full-rate clock C by aligning the phase and frequency of the divided clock C16 from the internal divider to the externally applied reference clock crp/crn. The divided clock is delivered to outputs c16p/c16n through a CML output buffer LS COB. Selection of the required VCO is defined by the CMOS control signals vc0 and vc1 as shown in Table 1. The same signals are used to activate the LS COB block. Here "nc" means "not connected".

Table 1. VCO and LS COB Control Modes

vc0	vc1	Selected VCO	LS COB
"0"	"0"	VCO1 (lower frequency)	On
"0"	nc	VCO1 (lower frequency)	Off
"0"	"1"	VCO2 (medium frequency)	On
nc	"0"	VCO3 (higher frequency)	Off
nc	nc	VCO1 (lower frequency)	Off
nc	"1"	VCO2 (medium frequency)	Off
"1"	"0"	VCO3 (higher frequency)	On
"1"	nc	VCO3 (higher frequency)	Off
"1"	"1"	VCO2 (medium frequency)	On

The PLL can also operate in open-loop mode with an external control voltage applied to pin fltr. In this case, the unused VCO is completely disabled in order to save power. The allowed control range is shown in Table 2.

Table 2. VCO Control Voltage

fltr voltage, *V*	Frequency of the active VCO
vcc	min
vcc-2.5	max

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HS COB

The High Speed Clock Output Buffer (HS COB) receives a full-rate clock C from the PLL and converts it into CML output signal cp/cn. The buffer provides an internal single-ended termination of 50*Ohm* to vcc for each output line and also requires 50*Ohm* external termination resistors to be connected between vcc and each output.

LS COB

The Low-Speed Clock Output Buffer (COB) receives the divided-by-16 clock signal from the PLL's divider and converts it into LVDS output signal c16p/c16n. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.5*GHz* with low power consumption. The buffer satisfies all requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. For correct operation, it requires external differential 100*Ohm* DC termination at the receiver side. The output pins should **NEVER be CONNECTED** to devices with 50*Ohm* termination to ground **WITHOUT DC BLOCKS!**

The buffer can be enabled or disabled by the external 3-state control signals vc0 and vc1 as shown in Table 1 above.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = -2.8*V* or −3.3*V*), or positive supply (vcc = +2.8*V* or +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all CML I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vee = 0.0*V* and vcc = +3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		3.6	*V*
Power Consumption		580	*mW*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	3	Output	CML differential clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
cn	5		
Low-Speed I/Os			
crp	17	Input	LVDS/CML clock inputs. See LS CIB for allowed application schemes
crn	15		
c16p	23	Output	LVDS clock outputs. See LS COB for a detailed description
c16n	21		
Controls			
vc0	9	Input	3-state control signals
vc1	11		
fltr	19	Input	Pin for connecting the external loop filter. Can be also used for VCO external control in open-loop mode

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+2.8*V* or +3.3*V*)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	External ground (0*V*)	1, 7, 13

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc		2.8 / 3.3		*V*	±5%
*I*vcc		160		*mA*	
Power consumption		450 / 530		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Reference Clock (crp/crn)					
Frequency	1.50		2.006	*GHz*	1/16 of the VCO frequency
Swing	200		800	*mV*	Differential, p-p
CM Voltage Level	1.2		vcc-0.4	*V*	
HS Output Clock (cp/cn)					
Frequency	24.0		32.1	*GHz*	Matches VCO frequency
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.55		*V*	
Jitter		200		*fs*	Peak-to-peak at 25.78*GHz*
Duty Cycle		50%			
Phase Noise		108		*dBc/Hz*	At 32*GHz* at 1.0*MHz* offset
LS Output Clock (c16p/c16n)					
Frequency	1.50		2.006	*GHz*	
Interface		LVDS			Meets the IEEE Std.
3-State control inputs (vc0, vc1)					
Logic “1” level	vcc-0.3			*V*	
“nc” level		(vcc+vee)/2			Recommended to keep not connected. The required level is created internally.
Logic “0” level			vee+0.3	*V*	
VCOs					
Low frequency of VCO1		24.0		*GHz*	Lower-frequency VCO
High frequency of VCO1		27.5		*GHz*	
Low frequency of VCO2		25.3		*GHz*	Medium-frequency VCO
High frequency of VCO2		27.7		*GHz*	
Low frequency of VCO3		27.5		*GHz*	Higher-frequency VCO
High frequency of VCO3		32.1		*GHz*	
External control voltage range	vcc-2.5		vcc	*V*	In open-loop mode

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

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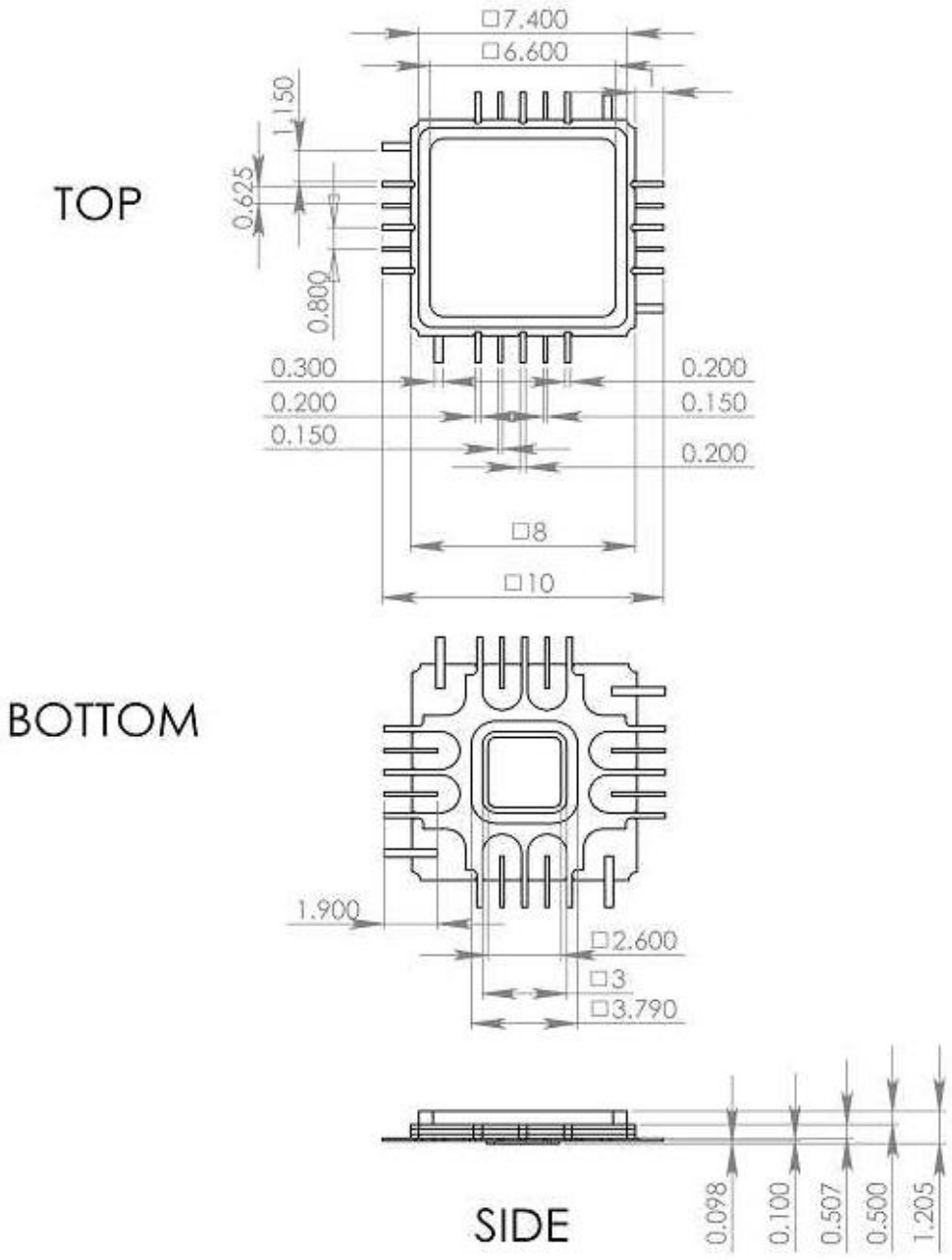

Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT8151-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.6.2	02-2020	Updated Package Information
1.5.2	07-2019	Updated Letterhead
1.5.1	08-2015	Updated External Filter Schematics Updated electrical characteristics Updated package information section
1.4.1	04-2015	Updated clock output jitter value
1.3.1	09-2014	Updated lower frequency of operation Updated lower frequency in electrical characteristics table
1.2.1	05-2013	Corrected title Corrected filter schematics Corrected power supply configurations Corrected electrical characteristics
1.1.1	04-2013	Corrected title Corrected electrical characteristics
1.0.1	03-2013	Initial release